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FAULT DIAGNOSIS IN ANALOG ELECTRONIC CIRCUITS – THE SVM APPROACH

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Abstract

In this paper, the application of the SVM (Support Vector Machine) algorithm has been used for diagnosis and tests of analog electronic circuits. The diagnosis procedure belongs to simulation-before-test techniques, where simulations of the circuit under test (CUT) are performed at the before-test stage. Two examples have been verified for parametric and catastrophic faults in the time domain, but the conclusion is driven with the use of assumed features. A fault-driven test (FDT) has been applied to a filter circuit and a specification-driven test (SDT) to a field-programmable analog array (FPAA). The SVM classifies features which are calculated from the time domain responses. Results obtained from the examples prove a high detection and localization level of circuit states with the use of the SVM classifier.

Keywords: fault diagnosis, electronic circuits, support vector machine SVM.

1. Introduction

The still-increasing concentration of elements in electronic devices causes a big issue for test and diagnosis. If high frequency systems or data acquisition systems are considered, then two parts, the analog and digital ones, must be diagnosed. Digital circuit diagnostics have well-defined test procedures. As distinct from the digital side, mixed and specially analog circuits do not have any standard diagnostic approaches [1, 2]. However, there are a few fundamental books which describe the process of diagnosis of analog, mixed and digital electronic circuits [3,4]. Modern electronics requires convenient and simple tools for diagnosis of analog circuits which are integrated on the same substrate with digital ICs. Testing of the mixed (analog and digital) electronic devices is obligatory due to the cost of production which increases drastically (usually 10 times) on the following level: wafer (less than 1 cent), package, module, system, field service (up to thousands of dollars). If a new mixed IC is designed, new methods for diagnosis and test are necessary. Therefore, detection of a bad specification, as quick as possible, is the main possibility to cut manufacturing costs [1, 3].

In case of digital testing, the IEEE1149.1 standard are well described and commonly used. For analog systems, there is lack of standards which are frequent in use. However, the researchers have proposed the mixed signal boundary path IEEE1149.4 [3].

Two different approaches to analogue circuit testing can be distinguished [1]:

1. Specification-driven test (SDT), where the system functionality is checked. The system under test must meet the device requirements in order to pass the SDT.
2. Fault-driven test (FDT), where the main purpose is to find a faulty component which usually causes system failure.

In the advance of integrated circuit (IC) technology, access to internal nodes is limited and specification-driven testing seems to be more practical. For FDT and SDT two techniques are possible: Simulation Before Test (SBT) and Simulation After Test (SAT) [1].

One of the major problems in the area of diagnosis is design for testability [5], where the test point selection [6, 7, 8] and the input source function [9, 10, 11] are optimized. For test point optimization an entropy measure is proposed in [7] and similar problem with use of genetic algorithm is described in [8]. The input source optimization can be divided into two domains. A piecewise linear (PWL) function is designed [12] in case of time domain and a multitone signal (sum of limited number of frequencies) is created in the AC domain [9, 10]. A heuristic algorithm of simulated annealing is proposed in [11] for optimal multitone selection. In case of the time domain, the output responses are acquired and classification is based on selected features (delay time, rise time, *etc*.) [12].

The problem of analog fault diagnosis is very complex due to tolerances of elements and mainly continuous domain of circuit specification. The other well-known facts come from the size of the analog part which occupies a much greater area than digital components. For a mixed IC, it is estimated that only 10% of the substrate consist of analog part but the diagnosis cost exceeds 80% of the whole validation process (both analog and digital tests). Typically, the analog part consists of less than 100 elements and is responsible for acquiring information from the surrounding world (*e.g.* MEMS) or/and performing pre-processing operations on the analog signal (*e.g.* antialiasing filter). The circuit responses are measured for the selected test nodes in the predefined domain. A DC analog fault dictionary determination is proposed in [13]. In order to enhance the accuracy of classification, a number of soft computing algorithms can be applied [14, 15, 16]. Another reason for applying fuzzy logic is the masking effect of analog elements which leads to an ambiguity region [3]. Historically, the ambiguity region equals 0.7V for DC domain circuits, which means if the voltage in a particular node for at least two circuit states is less then 0.7 then the states are not separable. Nowadays, researchers apply the Monte Carlo analysis more frequently in order to determine an ambiguity region for a test point [10, 12]. The idea of the ambiguity region is presented in Fig. 1.

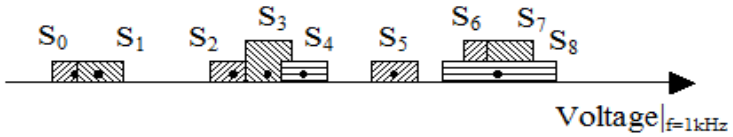

Fig. 1. Exemplary circuit states for voltage distribution and the frequency equals 1kHz .

According to Fig. 1, it is impossible to separate states: (S_0; S_1) and (S_2; S_3) and (S_3; S_4) because there is no free space between them. On the other hand, states (S_2; S_4) are separable. A fault represented by S_5 may be located by the use of single frequency (1kHz). Three other states S_6, S_7 and S_8 mask each other, so other test point or more frequencies are required to locate these faults.

There are a number of artificial intelligence (AI) classification methods [14, 17, 22] which provide significantly better classification results compared with the classical methods [13]. Aminian in [17] and Kuczyński in [20] propose a wavelet transform for pre-processing and justify better diagnosability of the electronic systems. More, a neural network is designated for the purpose of diagnosis of the single [17] and global parametric [22, 25] faults. Another technique for fault diagnosis has been proposed in [18], where measurements are transformed in multi-dimentional space. An algorithm for multiple fault diagnosis has been described in [21], the method is based on very precise measurements at test points.

The SDT for a field-programmable analog array (FPAA) is proposed in [19]. The authors present a diagnosis method with the use of the internal structure of the hardware. Hardware implementation of the built-in type test is proposed in [23, 24]. A very interesting approach is described by Toczek and Kowalewski in [23] which evaluates nonlinearities based on built-in test scheme.

The main disadvantage of AI algorithms is non deterministic behavior, which often leads to unacceptable deviation of results (an AI algorithm for exactly the same data creates two different, but good results). On the contrary, any deterministic method for the same input will create exactly the same output results [9, 14, 21].

Yet, the SVM algorithm [26-29] is applied for soft and hard faults diagnosis in analog electronic circuits. In this article, the time domain response for unit step excitation as well as soft and hard fault injection are considered. In the next paragraph the application of the SVM to analog fault diagnosis is presented. Next, two examples of different type are evaluated: the first one is simulated in a PSpice circuit simulator and the second one with the use of FPAA.

2. Application of the SVM algorithm to Analog Electronic Circuit Diagnosis

In this paragraph, the procedure for circuit diagnosis with use of the SVM algorithm is described. At the before-test stage, the following questions and statements have to be considered [1-3].

1. What are the fault types in the circuit? How is the type of fault modelled? How many faults occur simultaneously? Considering these questions, two types of faults have been assumed: soft and hard type of discrete elements. Soft (parametric) faults have been simulated as a 50% deviation greater and lower with respect to the nominal value. Hard (catastrophic) types of fault have been simulated by adding 10^{10} Ω resistance in series for open element or 10^{-2} Ω resistance in parallel for modeling a short. Basically, a single fault occurrence is investigated.
2. Define circuit states for all selected faults (hard and/or soft):

$$\mathbf{F}=\{f_0,\ldots,f_{S-1}\}, \tag{1}$$

where f_0 is a healthy state, S – the number of considered states.

The SVM algorithm is working for two classes, so S circuit states lead to N classification functions (see eq. 2 and 3) depending on test strategy.

   a. Detection of a single fault. A healthy state f_0 must be isolated from all other states. Then, the total number of decision functions is one:

$$N=1. \tag{2}$$

   b. Localization of a single fault. Yet, the SVM procedure must be divided into a few steps in order to classify the multi-class data. At the first stage, a particular class should be isolated from other classes. Then, the second class is separated from all other classes, etc. In order to perform multi-class classification, an N number of SVM set have to be learnt. The number of decision function can be obtained from the formula:

$$N = S\,, \tag{3}$$

where S is the number of circuit states.

3. What is the domain for diagnosis? A test engineer considers the DC, AC or time domain depending on the circuit structure, circuit behavior, or circuit performance. In this paper the time domain test has been applied, however the SVM algorithm can be applied in other domains.

Input signal in the time domain $u_{in}(t) = \mathbf{1}(t)$ which produces a response in a test point *i* $u_i(t)$. If the SBT stage is considered, then *S* simulations should be performed in order to calculate nominal values of characteristic parameters of the response for each circuit state. For that case the input and output signals create vectors of length *L*:

$$u_{in} = \left[u_{in}(t_1), u_{in}(t_2), ..., u_{in}(t_L)\right], \tag{4}$$

$$u_i = \left[u_i(t_1), u_i(t_2), ..., u_i(t_L)\right], \tag{5}$$

where *i=1,...,P* – the total number of accessible test points.

4. How many test points are accessible? For some systems, only input and output pins (gates) are free to measure. For other CUT, a bed of nails is mandatory in order to acquire signals from more test points, then a quite precise diagnostic can be performed. The presented method examines the output time domain response (*P=1*) for a unit step excitation:

$$u_1 = \left[u_1(t_1), u_1(t_2), ..., u_1(t_L)\right] = u_{out}. \tag{6}$$

5. Create an ambiguity region for all circuit states by analyzing a number (*M*) of Monte Carlo runs for each circuit state responses in time domain which create a set of responses for a circuit state f_i:

$$\mathbf{u}_{out}^{(f_i)} = \left[u_{out,1}^{(f_i)}, u_{out,2}^{(f_i)}, ..., u_{out,M}^{(f_i)}\right]. \tag{7}$$

The upper and lower envelopes of the output responses are calculated based on eq. (7):

$$\mathbf{u}_{out,upper}^{(f_i)} = \left[\max\left\{u_{out,i}^{(f_i)}(t_1)\right\}, \max\left\{u_{out,i}^{(f_i)}(t_2)\right\}, ..., \max\left\{u_{out,i}^{(f_i)}(t_L)\right\}\right],$$

$$\mathbf{u}_{out,lower}^{(f_i)} = \left[\min\left\{u_{out,i}^{(f_i)}(t_1)\right\}, \min\left\{u_{out,i}^{(f_i)}(t_2)\right\}, ..., \min\left\{u_{out,i}^{(f_i)}(t_L)\right\}\right],$$

where *i=1, ..., M*.

6. Select features of the time response for evaluation and classification. It is much easier and more convenient to evaluate a reduced number of data (features) than vectors acquire in the time domain (usually thousands of points). A feature is calculated for each circuit state considered which gives characteristic values of all selected features (maximum, minimum and nominal):

$$\mathbf{A}^j = \left[\mathbf{A}_1, \mathbf{A}_2, ..., \mathbf{A}_T\right], \tag{8}$$

where each feature is described by three characteristic values for a state *j*:

$$\mathbf{A}_i = \left\{A_i^{nom}, A_i^{\max}, A_i^{\min}\right\} \tag{9}$$

and *T* is a number of features selected for all states.

Exemplary features in time domain are: rise time of the first extreme, number of extremes, derivative of the rise time, overshoot, etc. Because the MC analyses are performed, the maximum, minimum and nominal values for each attribute can be formulated. The features are linked with the circuit states and then the SVM algorithm builds decision functions based on selected features. Some typical features are as follows:

– $A_1 = u_{out}(t_{const})$ – voltage value for time t_{const};

– $A_2 = u_{out}(t_i)$: $\dfrac{u_{out}(t_i) - u_{out}(t_{i-1})}{t_i - t_{i-1}} > 0 \wedge \dfrac{u_{out}(t_i) - u_{out}(t_{i+1})}{t_i - t_{i+1}} < 0$ – voltage value of the first maximum (overshoot);

– $A_3 = t_i : \frac{u_{out}(t_i) - u_{out}(t_{i-1})}{t_i - t_{i-1}} > 0 \wedge \frac{u_{out}(t_i) - u_{out}(t_{i+1})}{t_i - t_{i+1}} < 0$ – time of the first maximum;

– $A_4 = \max\{u_{out}(t_i)\}$ – maximum voltage value;

– A_5 = voltage difference between two first extremes;

– A_6 = time difference between two first extremes;

– A_7 = gradient value [*V/s*], the slope of the characteristic.

– $A_8 = d_f$ damping factor of decaying oscillations, which is calculated as follows:

$$\left.\begin{aligned} Ae^{-\frac{t_1}{d_f}} &= V_1 \\ Ae^{-\frac{t_2}{d_f}} &= V_2 \end{aligned}\right\} \rightarrow d_f = \frac{t_2 - t_1}{\ln\left(\frac{V_1}{V_2}\right)}. \tag{10}$$

The values V_1 and V_2 are measured for two peaks, as can be seen in Fig. 2.

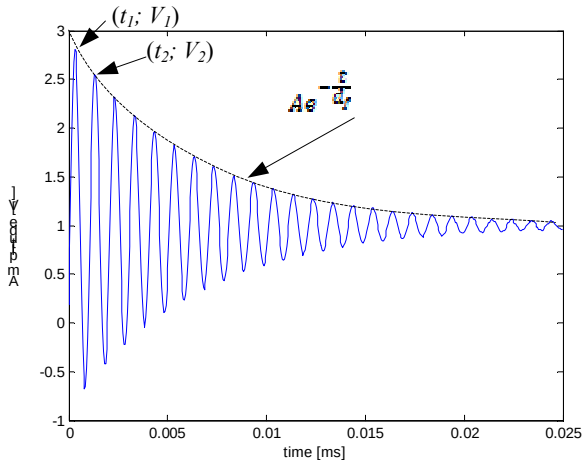

Fig. 2. Calculation of the damping factor.

Obviously, a limited number of features occurs for a circuit under test, *i.e.* the damping factor of oscillations cannot be observe in the first-order circuits.

7. Create decision functions with use of the SVM algorithm. The main goal of the SVM algorithm [26, 29] is to create *N* decision functions (classifier) which will separate data points belonging to constant number of classes (*S* – number of classes). The SVM algorithm has a number of advantages: it is deterministic and creates an optimal sub-plane which separates data points from different classes. They are currently the best-known classifiers on a well-studied hand-written-character recognition benchmark [26].

To make the method robust, two features out of T have been taken into consideration during a single optimization process. Decision functions have been designed for a pair of features which have been chosen from set **A**={*A'*,*A''*}. A number of classifiers relate to the level of diagnosis, and it is described by a number of *N* (see eq. 2 and eq. 3). As mentioned before, the HTRBF (Heavy Tailed Radial Basis Function) kernel function has been utilized in the SVM algorithm which gives two more parameters and degrees of freedom, namely *a* and *b*. Based on the *a, b* parameters and chosen features, the test designer decides what the best features and parameters *a, b* are. Both parameters are chosen experimentally for presented later benchmarks.

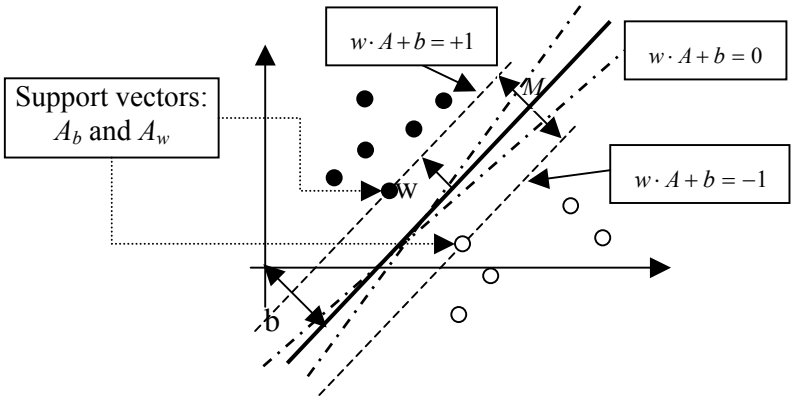

Fig. 3. Linear classifier for two classess in two dimensional plane.

In order to construct the SVM classifier, a number M of Monte Carlo analyses for each state have to be simulated. Yet, the total number D of a feature A' is a product of M analyses and circuit states S ($D=MS$).

Let us consider a linear separable problem. According to Fig. 3, there can be an infinite number of classification function (solid and dash-dot lines) but only one will satisfy the maximum margin distance M between two classes (solid one). The boundary and margin lines can be defined:

For class „black" (can be considered for damaged circuits): $\{\mathbf{A} : w \cdot \mathbf{A} + b = +1\}$. (11)

For class "white" (can be considered for healthy circuits): $\{\mathbf{A} : w \cdot \mathbf{A} + b = -1\}$. (12)

For points within margin: $\{\mathbf{A} : -1 < w \cdot \mathbf{A} + b < +1\}$, (13)

where: $\mathbf{A}$ – is a vector of features, w – is perpendicular to the "black" and "white" lines. So, the problem is to find the solution to the following system of equations:

$$\begin{aligned} & w \cdot \mathbf{A^b} + b = +1 \\ & w \cdot \mathbf{A^w} + b = -1 \\ & \mathbf{A^b} = \mathbf{A^w} + \lambda \mathbf{w} \\ & \left| \mathbf{A^b} - \mathbf{A^w} \right| = M \\ & \lambda = \frac{2}{\mathbf{w} \cdot \mathbf{w}}. \end{aligned} \tag{14}$$

If the number of data is D then the number of constraints is also D. If we assume a data set:

$$\left(\mathbf{A}_k ; y_k\right) \quad where \quad y_k = \pm 1 \quad and \quad k = 1, ..., D. \tag{15}$$

Then constraints are described as follows:

$$\begin{aligned} & w \cdot \mathbf{A}_k + b > +1 \ \text{ for } \ \mathrm{y_k} = +1 \\ & w \cdot \mathbf{A}_k + b < -1 \ \text{ for } \ \mathrm{y_k} = -1. \end{aligned} \tag{16}$$

Now, any method, like quadratic programming (QP), can be utilized in order to find the maximum margin M in terms of $\mathbf{w}$ and b. The quadratic optimization criterion is:

$$\min w \cdot w \tag{17}$$

QP is a well-studied class of optimization algorithms to maximize a quadratic function of some real-valued variables subject to linear constraints [22]. It works very well if all data points are in the correct half-plane. However, the above example is very simple to understand, but not realistic. Real world systems do not offer data which are linearly separable. Hence,

there is no opportunity to create a linear decision function for dividing the space into two classes with 100% efficiency. For this reason, the parameter C (distance of error points to their correct place) responsible for a misclassification measure has been introduced to the SVM algorithm [4, 24]. According to (15), there is still the same amount of data but linearly inseparable (assume data with noise). For this case, the constraints equations are:

$$\begin{aligned} & w \cdot \mathbf{A}_k + b > +1 - \varepsilon_k \quad \text{for } \mathrm{y_k} = +1 \\ & w \cdot \mathbf{A}_k + b < -1 + \varepsilon_k \quad \text{for } \mathrm{y_k} = -1 \\ & \underset{k}{\forall} \varepsilon_k \geq 0. \end{aligned} \tag{18}$$

So, the number of constraints increases to *2D* and the quadratic optimization criterion is changed into:

$$\min\left[\frac{1}{2} w \cdot w + C \sum_{k=1}^{D} \varepsilon_k\right]. \tag{19}$$

Another important property of the SVM flows from its kernel function, which allows transformation of the input space into a feature one. Non-linear mapping gives amplification of important features and attenuation of insignificant ones. Usually, the kernel mapping function causes linearity of the input problem in a new, higher dimension, space [28].

In order to find the optimal separating function, the following optimization problem has to be solved:

$$\text{maximize}\left(\sum_{k=1}^{D} \alpha_k - \frac{1}{2} \sum_{k=1}^{D} \sum_{l=1}^{D} \alpha_k \alpha_l y_k y_l \Phi(\mathbf{A}_k, \mathbf{A}_l)\right), \tag{20}$$

where:

- α – Lagrange multipliers;
- y – classes, *e.g.* $y = \{0,1,2,3,...,S-1\}$,
- $\Phi(\mathbf{A}_k, \mathbf{A}_l)$ – kernel function, *e.g.* HTRBF:

$$\Phi(\mathbf{A}_k, \mathbf{A}_l) = e^{-\rho \left| \mathbf{x}_k^a - \mathbf{x}_l^a \right|^b}, \tag{21}$$

where a, b are parameters and ρ=1.
Subject to the following constraints:

$$0 \leq \alpha_k \leq C, \quad k = 1,2,\ldots,D, \tag{22}$$

$$\sum_{k=1}^{D} \alpha_k y_k = 0, \tag{23}$$

where: C is the measure of misclassification, D is the number of training data. Datapoints with α_k>0 are the support vectors.

Afterwards, two parameters have to be defined:

$$\begin{aligned} & \mathbf{w} = \sum_{k=1}^{D} \alpha_k y_k \mathbf{A}_k \\ & b = y_K \left(1 - \varepsilon_K\right) - \mathbf{A}_K \mathbf{w}_K, \end{aligned} \tag{24}$$

where: $K = \arg\max_k \alpha_k$.

Then the classification function is done with:

$$f(\mathbf{A}, \mathbf{w}, b) = \mathrm{sgn}(\mathbf{w} \cdot \mathbf{A} - b). \tag{25}$$

3. Computational Examples

The procedure presented in the previous section has been implemented in Matlab environment as m-files. Pspice [27] has been called from m-scripts in order to perform simulations of the exemplary circuits for all states considered. 100 Monte Carlo simulations have been performed for each state.

3.1. Example 1

Considering circuit in Fig. 4, a fault driven test has been applied and the following hard and soft faults have been assigned:

- F_{hard}={*fault-free; R1*$_{open}$; *R1*$_{short}$; *R2*$_{open}$; *R2*$_{short}$; *RA*$_{open}$; *RA*$_{short}$; *RB*$_{open}$; *RB*$_{short}$; *C1*$_{open}$; *C1*$_{short}$},
- F_{soft}={*fault-free; R1*$_{high}$; *R1*$_{low}$; *R2*$_{high}$; *R2*$_{low}$; *RA*$_{high}$; *RA*$_{low}$; *RB*$_{high}$; *RB*$_{low}$; *C1*$_{high}$; *C1*$_{low}$}.

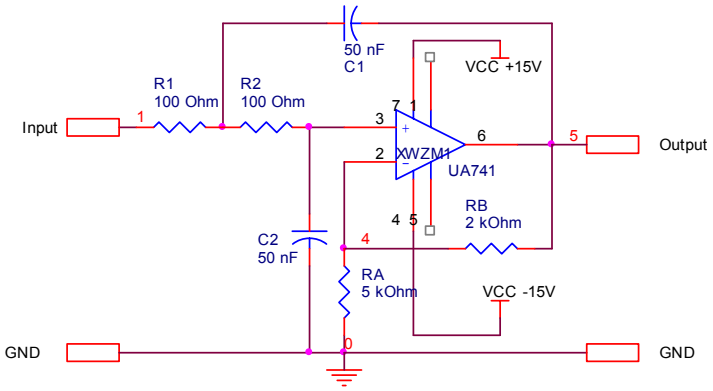

Fig. 4. Example 1.

The aforementioned parametric and catastrophic faults in all passive elements have been investigated, where subscripts:

- *short* – parallel resistor with "short" element of 10^{-2} Ω;
- *open* – series resistor with "open" element of 10^{10} Ω;
- *low* – nominal value of a particular element multiplies by 0.5;
- *high* – nominal value of an element multiplied by 1.5.

Tolerances of undamaged elements are as follows: capacitor tolerance is 3% and resistor tolerance is 5%.

The circuit has been driven by unit step excitation and responses have been measured at the output node. Fig. 5 presents circuit responses for exemplary parametric faults and the healthy circuit response (thicker line). Next, a set of features $A=\{A_1,...,A_8\}$, based on the output response, have been selected:

- $A_1=V_{t1}$ voltage value for time t_1=350 μs (steady state value);
- $A_2=V_{t2}$ voltage value for time t_2=34 μs (first maximum occurrence for nominal response)
- $A_3=V_{max1}$ voltage value of the first maximum (overshoot);
- $A_4=t_{max1}$ time of the first maximum;
- $A_5=V_{max}$ maximum voltage value;
- $A_6=\Delta V_{max1}$ voltage difference between two first extremes;
- $A_7=\Delta t_{max1}$ time difference between two first extremes;
- A_8=gradient value [V/s], the slope of the characteristic.

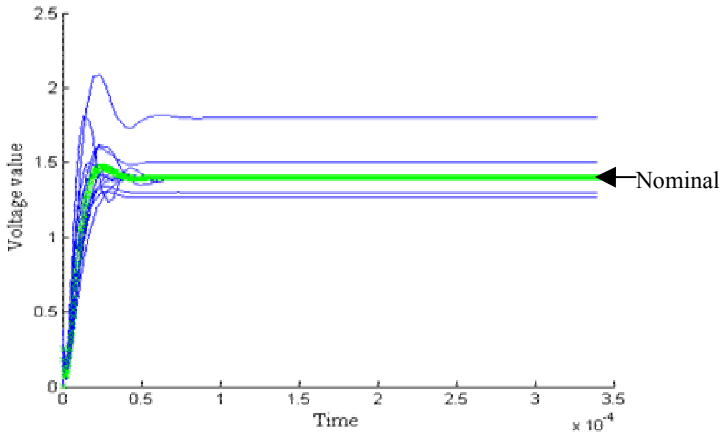

Fig. 5. Circuit responses for parametric faults.

Two sets of features have been arbitrarily selected, first for catastrophic faults classification $\mathbf{A_{cat}}=\{A_1, A_2, A_3, A_4, A_5\}$ and the second set for parametric faults classification $\mathbf{A_{soft}}=\{A_1, A_6, A_7, A_8\}$.

Using MC analysis, the boundary values of all features from set $\mathbf{A_{cat}}$ and $\mathbf{A_{soft}}$ with respect to each circuit state F_{hard} and F_{soft} have been designated and gathered in Table 1 and 2, respectively. The boundary values for each circuit state give the possibility to define an insensitive margin, where a particular state cannot be isolated from the other if both deviations overlap each other. The nominal point of the state (pattern) is defined by the nominal values of features.

Values included in both Tables 1 and 2 have been utilized for building SVM classifiers. Each fault (circuit state) is represented by three characteristic values of every feature. There are many kernel functions; however, we have chosen the HTRBF function because of the complex character of input data and good enough properties. The kernel function requires two parameters a and b while processing the decision function. The parameters should be adjusted during the learning process in order to receive the best-quality classification. There is no common principle for determination of a and b, so we have to limit the universe for both parameters within 0.1 and 2 with a step of 0.1. All combinations of parameters a and b have been checked and selected together with the obtained results; they are presented in Tables 3 and 4 for catastrophic and parametric fault localization, respectively.

A detection graph for two features has been shown in Fig. 6. It indicates two circuit states: a healthy (in the middle) and all damaged ones with respect to features A_2 and A_4. Between these classes (states) an ambiguity region exists where the correct assignment is impossible, however incorrect classification is less then 1%.

Figs 7 and 8 present the localization of catastrophic faults in a two-dimensional plane, namely feature A_3 versus feature A_4. In order to clarify Fig. 7, the rectangular area is zoomed and shown in Fig. 8. There is not only one area for some circuit states, which means they cannot be grouped into one “solid” area with the use of the features presented. It is very good behavior of the SVM algorithm because classic algorithms of data mining (like the nearest neighbourhood method) tries to group all similar patterns.

Table 1. Characteristic values of features for selected catastrophic faults.

	Feature	***R1$_{short}$***	***R1$_{open}$***	***RA$_{short}$***	***C1$_{short}$***	***C2$_{open}$***	***healthy***
Nominal value	A_1 [V]	-13,5	1,4	14,1	1,4	0,002	1,4
	A_2 [V]	-13,5	1,39	14,1	1,36	0,001	1,44
	A_3 [V]	0	1,2	14,1	1,4	0,005	1,47
	A_4 [µs]	0	35	Inf	Inf	51	76
	A_5 [V]	-13,5	1,41	14,3	1,4	0,247	1,47
Minimum value	A_1 [V]	-13,5	1,34	14,1	1,33	0,002	1,33
	A_2 [V]	-13,5	1,32	14,1	1,28	0,001	1,36
	A_3 [V]	0	1,1	14,1	1,33	-0,01	1,37
	A_4 [µs]	0	34	Inf	123	29	63
	A_5 [V]	-13,5	1,34	14,2	1,33	0,226	1,37
Maximum value	A_1 [V]	-13,4	1,48	14,1	1,47	0,002	1,48
	A_2 [V]	-13,4	1,47	14,1	1,44	0,002	1,51
	A_3 [V]	0	1,27	14,1	1,47	0,005	1,58
	A_4 [µs]	0	38	Inf	Inf	63	89
	A_5 [V]	-13,4	1,5	14,3	1,47	0,27	1,58

Table 2. Characteristic values of features for selected parametric faults.

	Attribute	***R1$_{low}$***	***R1$_{high}$***	***RA$_{low}$***	***C1$_{high}$***	***healthy***
Nominal value	A_1 [V]	1,4	1,4	1,8	1,4	1,4
	A_6 [V]	1,29	1,41	1,98	1,54	1,4
	A_7 [µs]	53	80	65	62	70
	A_8 [V/s]	0,03	0,03	0,05	0,03	0,03
Minimum value	A_1 [V]	1,34	1,34	1,72	1,33	1,33
	A_6 [V]	1,23	1,32	1,8	1,42	1,3
	A_7 [µs]	45	72	49	57	58
	A_8 [V/s]	0,03	0,02	0,04	0,02	0,03
Maximum value	A_1 [V]	1,48	1,48	1,88	1,47	1,48
	A_6 [V]	1,39	1,54	2,2	1,7	1,49
	A_7 [µs]	72	96	71	83	83
	A_8 [V/s]	0,04	0,03	0,06	0,04	0,04

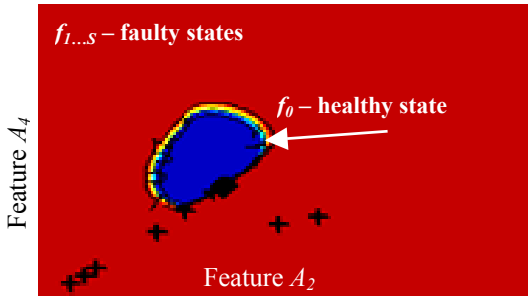

Fig. 6. Detection graph for catastrophic faults.

The final conclusion of the presented procedure is a pair of features and parameters *a*, *b* of the HTRBF kernel function which gives the best diagnostic results. An exemplary set of features and parameters for detection is shown in Tables 3 and 4 for catastrophic and parametric faults respectively. Obviously, all combinations of two features have been evaluated but only the chosen ones are listed in Tables 3 and 4. The classification results for other combinations are worse than presented.

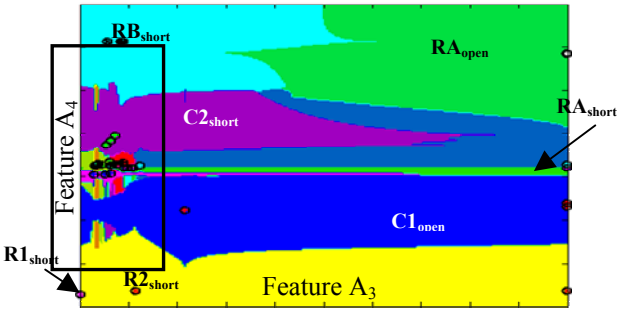

Fig. 7. Diagnosis plane for selected catastrophic faults.

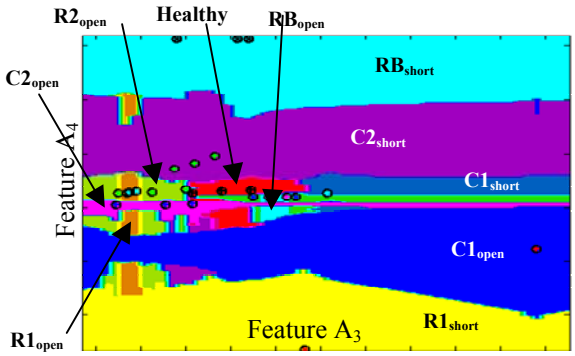

Fig. 8. Area selected in Fig. 7

Table 3. Results obtained for detection (localization) of catastrophic faults.

Features		***HTRBF parameter a***	***HTRBF parameter b***	***Classification results***	
				Detection [%]	***Localization [%]***
A_1	A_2	1,0 (0,8)	2,0 (2,0)	96,1	48,1
A_1	A_3	0,7 (0,2)	2,0 (2,0)	98,4	70,5
A_1	A_4	0,1 (0,3)	1,2 (0,2)	94,6	90,8
A_1	A_5	0,4 (0,2)	2,0 (2,0)	88,4	64,6
A_2	A_3	0,9 (0,1)	2,0 (2,0)	87,0	72,3
A_2	***A_4***	0,1 (0,1)	2,0 (1,2)	**99,2**	81,3
A_2	A_5	0,1 (0,1)	1,2 (2,0)	78,3	66,1
A_3	***A_4***	0,1 (0,1)	1,2 (0,4)	91,5	**99,2**
A_3	A_5	0,1 (0,1)	1,4 (2,0)	82,5	70,1
A_4	A_5	0,1 (0,1)	1,8 (0,4)	98,3	92,0

Table 4. Results obtained for detection (localization) of parametric faults.

Features		***HTRBF parameter a***	***HTRBF parameter b***	***Classification results***	
				Detection [%]	***Localization [%]***
A_1	A_2	0,1 (0,3)	1,4 (2,0)	71,3	20,0
$\boldsymbol{A_1}$	$\boldsymbol{A_3}$	0,5 (0,2)	1,8 (2,0)	**80,8**	34,7
$\boldsymbol{A_1}$	$\boldsymbol{A_4}$	1,0 (0,7)	1,8 (1,0)	80,5	**52,2**
A_2	A_3	0,6 (0,1)	2,0 (0,4)	76,6	52,2
A_2	A_4	0,5 (0,9)	2,0 (2,0)	71,8	30,0
A_3	A_4	0,6 (0,1)	2,0 (1,0)	74,2	36,7

Each row of the table consists of two features, parameters *a* and *b* for HTRBF kernel and efficiency of detection and localization. Columns with parameters *a* and *b* have two values, where the first one is related to detection and the value in brackets refers to localization. Classification results are determined on the basis of 100 Monte Carlo simulations for each circuit state.

The test engineer can choose a pair of features which gives best accuracy in testing and diagnosis for parametric and catastrophic faults. In case of catastrophic faults, the best accuracy for testing is given by features: A_2, A_4 while for localization: A_3 and A_4. In case of parametric faults, the highest accuracy is given by features: A_1 and A_3. Finally, for localization of soft faults A_1 and A_4 have been chosen. The worst diagnostic results have been obtained for features A_6, A_7, A_8 and therefore they are not printed in the tables.

3.2. Example 2

The second example has been created in the field programmable analog array (FPAA) as a fourth-order circuit which has been composed with three blocks:

- low pass bilinear filter (LPF) of 100 kHz cutoff frequency – first-order circuit;
- band stop biquadratic filter (BSF) of 50 kHz notch frequency and quality factor of 1 – second-order circuit;
- high pass bilinear filter (HPF) of 10 kHz cutoff frequency – first-order circuit.

The circuit is presented in Fig. 9, where the aforementioned three blocks are excited by a step function and the time domain responses after each block are shown with the use of the built-in oscilloscope. The main aim of the example is to separate a non-faulty circuit state, which is represented by nominal values of all blocks within all other states based on the output response in the time domain. Parameter variation of all blocks is gathered in Table 5.

According to the output time-domain response, similar features have been selected, namely $A_{1\text{-}8}$. Now, we consider specification-driven test based on the set of features for two different approaches:

1. Detection of a healthy state (nominal values of all blocks) from all other states. Hence, the circuit states are: $F_1=\{CUT^{healthy};\ CUT^{faulty}\}$. The circuit is considered as healthy if and only if:
$$CUT^{healthy} = \left\{ f_0^{LPF} = 100\,kHz,\ f_0^{BSF} = 50\,kHz,\ f_0^{HPF} = 10\,kHz,\ Q^{BSF} = 1 \right\}.$$
2. Localization of a healthy block (nominal values of a single block) from all other states:
$$F_2=\{CUT^{healthy};\ LPF^{healthy};\ BSF^{healthy};\ HPF^{healthy};\ fault(s)\},$$
where:
$$LPF^{healthy} = \left\{ f_0^{LPF} = 100\,kHz \right\},\quad BSF^{healthy} = \left\{ f_0^{BSF} = 50\,kHz, Q^{BSF} = 1 \right\},\quad HPF^{healthy} = \left\{ f_0^{HPF} = 10\,kHz \right\}.$$

According to Table 5, the number of combinations flows from the range and step of considered circuit parameters (5 values for each frequency and 3 values of the quality factor) and it equals $3 \cdot 5^3 = 375$. A total of 375 configurations have been performed and only one

combination satisfies $CUT^{healthy}$ for detection. Similar for localization, where 4 circuit combinations should be isolated from the rest of simulations.

Then, the SVM algorithm has been applied and the results for detection and localization are:

1. The healthy state can be isolated with the use of two features: $\{A_1\ A_2\}$ or $\{A_1\ A_3\}$ or $\{A_1\ A_4\}$ or $\{A_2\ A_3\}$.
2. All blocks have been localized correctly with features: $\{A_1\ A_2\}$ or $\{A_1\ A_3\}$ or $\{A_2\ A_4\}$ or $\{A_3\ A_4\}$.

Fig. 9. Exemplary circuit built in FPAA and simulation results for nominal parameters.

The results obtained prove correct diagnosis with the use of the presented features together with the SVM algorithm. Thus, a 100% efficiency has been achieved for the aforementioned features. Once again, features $A_{6\text{-}8}$ do not give good enough accuracy for diagnosis, however for other circuits they might carry important diagnostic information.

Table 5. Characteristic parameters of blocks for example 2.

Block / Param.	LPF				BSF				HPF			
	Min	Nom	Max	Step	Min	Nom	Max	Step	Min	Nom	Max	Step
f_0 [kHz]	80	100	120	10	30	50	70	10	5	15	25	5
Q[-]	Not concerned				0.5	1	1.5	0.5	Not concerned			

4. Conclusions

The application of the SVM algorithm to fault diagnosis in analog electronic circuit has been presented in this paper. The SVM has been applied for the fault-driven test (FDT) and the specification-driven test (SDT). For FDT a filter has been investigated for both, parametric and catastrophic faults in all passive elements. Detection and localization of a single fault give an accuracy of more than 90% and 70%, respectively. In case of SDT, FPAA with predefined configuration has been considered and again, detection and localization of selected states are correct with the use of the features proposed. The weakest point of the applied procedure is determination of the kernel function and automatic selection of features. Moreover, for a kernel function some additional parameters should be usually defined. Unfortunately, there is lack of algorithms which can be introduced in order to set not even the best kernel function but also its parameters. On the other hand, it gives another degree of freedom for test engineer who can manipulate with the aforementioned parameters based on his experience for the best diagnosis results. Nevertheless, the classification of CUT states with use of the SVM algorithm is very effective and can be applied in a real environment by vendors because it classifies circuit states unequivocally and takes into account tolerances of

elements and after all it is a deterministic method. In other words, the classifier produces exactly the same decision functions for exactly the same input vectors. The inaccuracy can be further reduced by using other kernel functions and it will be under research in the future.

Contrary to artificial intelligence methods like neural networks, there is no influence of the training process on the final result which is very important behavior from a practical point of view. The algorithm is to be applied in the real environment with use of the analog tester that will be built by the authors in the future.

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